Profile

Name of the Faculty	Ganti. Sreelakshmi
Designation	Associate Professor
Department	Electronics and Communication Engineering
Area of Interest	Digital Systems, VLSI, Embedded Systems, Computer Architectures, Quantum Computing
Subjects Taught	PDC,STLD,DD,MPMC,MPI,ES,ESD,VLSI Design, SOC Architectures, CPLD and FPGAs, Low Power VLSI Design, DSD, Computer Networks, Advanced Microprocessors, PIC microcontrollers, DDVH
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Educational Qualifications:

S. No.	Degree	Specialization	University/College	Year
1.	DECE	ECE	Govt.Polytechnic for	1996

			women's, Cuddapah	
2	B.Tech	ECE	JNTU, Anantapur	2001
3.	AMIE	EEE	Institute of Electrical and Electronics, Kolkata	2002
4.	ME	Digital Systems	Osmania University, Hyderabad	2008

Paper Publications:

S. No.	Publication details
1	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**Hybrid Signed Digit Parallel And Multi Operand BCD Adders**" International Conference ICIDEST 17th& 18th April 2018, KCG college of Engineering and Technology, Chennnai. *(Conference is attached to SCI journalsaccepted for IJPAM yet to be published)*
2	G.Sree Lakshmi, Mohammad Salman, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**Efficient Vedic Signed Digit Decimal Adder**" Fourth International Conference on Devices, Circuits and Systems (ICDCS'18)ISBN: 978-1-5386-3476-9/18/$31.00 ©2018 IEEE 16th & 17th Mar 2018, Electronics and Communication Engineering Karunya Institute of Technology and Sciences
3	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**A Novel Approach to The Learning Of Vinculum Numbers In Two's Compliment Method For BCD Arithmetic Operations**"Proceedings of

	the Second International Conference on Computing Methodologies and Communication (ICCMC 2018)IEEE Conference Record # 42656; IEEE Xplore ISBN:978-1-5386-3452-3978-1-5386-3452-3/18/$31.00 ©2018 IEEE 475
4	G.Sree Lakshmi "**Floating point Vedic multiplier using Parallel prefix adders for Signal Processing Applications"** "International Conference on Recent Innovations in Electrical Electronics and Communications Systems RIEECS-2017", Graphic Era University, Dehradun during 28th and 29th Oct 2017.
5	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi"**Implementation of High Speed Vedic BCD Multiplier using Vinculum Method**" TENCON IEEE conference 22nd to 25th Nov 2016. 978-1-5090-2597-8/16/$31.00 c 2016 IEEE
6	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**Compressor Based 8x8 Bit Vedic Multiplier using Reversible Logic**" in the 3rd International Conference on Devices, Circuits and Systems (ICDCS'16) held from 3rd to 5th March 2016 at Karunya University, Coimbatore, India.978-1-5090-2309-7/16/$31.00©2016 IEEE
7	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**Compressor Based 8x8 Bit Vedic Multiplier using Reversible Logic**" in the 3rd International Conference on Devices, Circuits and Systems (ICDCS'16) held from 3rd to 5th March 2016 at Karunya University, Coimbatore, India.978-1-5090-2309-7/16/$31.00©2016 IEEE

8	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi"**Area_Delay_Power Efficient Booth Encoded Reversible Multiplier using Compressors**" 4th International Conference on Innovations in Electronics and Communication Engineering (ICIECE-2015),August 21st -22nd 2015, Hyderabad, India. ISSN 2249-9946 Vol 5 issue 2
9	G. Sree Lakshmi, Dr.B.K.Madhavi"**Design and Implementation of Low Power Reversible Wallace Tree Multiplier using Compressors For High Speed Applications**" at National Conference on Circuits, Signals and Systems during 22nd to 24th January, 2015 at Muffakam Jah College of Engineering and Technology, Hyderabad, India.ISBN:978-93-82570-47-9.
10	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi"**Design and Implementation of Vedic Multiplier using Reversible Logic**" at Third National Conference on Latest Trends in Signal Processing VLSI and Embedded Systems during June 2014, at Geethanjali College of Engineering and Technology,Hyd,India. ISBN978-93-83459-63-6, 2014,Bonfring
11	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**A High Speed Low Power Multiplier-Accumulator Architecture using Higher Radix Modified Booth Algorithm**" at 2nd World Conference on Applied Sciences, Engineering & Technology (WCSET 2013)
12	G.Sree Lakshmi, Dr.B.K.Madhavi "**Various Design Algorithms and Hard Ware Approaches to Decimal Floating Point Multipliers: *A***

	Comparative Analysis" IEEE International Conference ICARET-2013 8th& 9th Feb 2013 at K L University, Vijayawada, India.
13	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**A Review of Low Power and High Performance Multipliers and Their Hardware Implementations**" presented at RITS International Conference on Advancements in Engineering and Management during 28th and 29th Feb 2012 at Hyderabad, India.
14	**INTERNATIONAL JOURNALS:** G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**Efficient Realization of Vinculum Vedic BCD Multipliers for High Speed Applications**" in Journal of Circuits and Systes,2018,vol 9, with ISSN 2153-1293 , DOI:10.4236/cs.2018.96009 June 2018.
15	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**Hybrid Signed Digit Parallel and Multi Operand BCD Adders**" ICIDEST 17th& 18th April 2018, KCG college of Engineering and Technology, Chennai
16	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi"**Implementation of High Speed Vedic BCD Multiplier using Vinculum Method**" TENCON IEEE conference 22nd to 25th Nov 2016. 978-1-5090-2597-8/16/$31.00 c 2016 IEEE Publisher: IEEE Digital Xplorer
17	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi "**Compressor based 8x8 Bit Vedic Multiplier using Reversible Logic**" in the 3rd International Conference on Devices, Circuits and Systems (ICDCS'16)

	held from 3rd to 5th March 2016 at Karunya University, Coimbatore, India. 978-1-5090-2309-7/16/$31.00©2016 IEEE. Publisher: IEEE Digital Xplorer.
18	G.Sree Lakshmi, Dr.Kaleem Fatima, Dr.B.K.Madhavi"**Area_Delay_Power Efficient Booth Encoded Reversible Multiplier using Compressors**" Journal of Innovation in Electronics and Communication Engineering(An International Journal) Jul-Dec 2015 Volume5, Issue2 ISSN: 2249-9946.
19	G.Sree Lakshmi, Dinesh Alapati Dr.Kaleem Fatima, Dr.B.K.Madhavi "**High Performance BCD Adder-Subtractor Using Reversible Logic**" International Journal of Engineering Inventions Nov-Dec 2012 ISSN: 2278-7461.

Books/Book Chapters Published:

S. No.	Publication details
1	A Frame work for Decimal Floating point Multiplier using Vinculum Multipliers G.Sree Lakshmi, Kaleem Fatima, B.K.Madhavi Science Direct International 2021, Chapter 11 DOI:10.9734/bpi/nips/v13/6866D Feb, 2021

Experience:

Teaching	18 years
Industry	1 year

Research	------
Total Experience	19 years